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Design of two-dimensional photonic crystal based optical NOT gate using square photonic crystal cavity

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***Abstract*: Using a square photonic crystal cavity,anovel design that replicates an optical NOT gate at an operating wavelength of $1.55\ \mu m$is presented. The proposed gate has a very small footprint, measuring only a few micrometers square. The contrast ratio is $7.69\ dB$, and the response time is $150\ fs$. The operation of the suggested device is investigated using a 2D-FDTD approach.**

Keywords— Photonic Crystal, Not Gate.

I. INTRODUCTION

Photonic crystals (PhCs) are a periodic dielectric structure consisting of two different dielectric materials with different dielectric constants [1-2]. It has a unique optical property called a photonic band gap (PBG) as a result of its periodicity [3]. The PBG is a frequency or wavelength band that is not permitted to propagate into the PhC [3]. PBG features and manipulation have been employed in the design of a variety of optical components and devices [4], including optical logic gates, filters, decoders [5-13], set reset latches [14], and so on.

In all these, optical logic gates are used in optical communication networks and high-information processing applications [15]. It's also used for rutting and switching optical signals between optical channels.

In the present study, an optical NOT gate employing a square photonic crystal cavity (SPhCC) is proposed. Itworks based on interference effect [8]. The utility of suggested NOT gate is demonstrated utilizing 2D-finite-difference time-domain i.e. 2D-FDTD technique [2,16]. Accurate Matched Layers (PMLs) in all side of simulating areas are used to modify the unbounded space to explore the behaviour of the wave and defective modes [17]. The structure's dispersion diagram is calculated using the Plane Wave Expansion (PWE) numerical method [17-18]. In terms of footprint and response time,the proposed structure is good.

II. STRUCTURE DESIGN

2D square lattice of Silicon rods in air has been suggested and designed. To operate the optical NOT gate in the third optical window, the refractive index of silicon is estimated to be 3.46 for the $1.55\ \mu m$wavelength. The radius of dielectric circular rods is chosen to be $0.2\ \times a$, Here the value of a (lattice constant of PhC structure) is 558 nm,

The optical NOT gate is designed by the use of square PhC cavity (Fig. 1). In SPhCC design,12 dielectric rods of radius 51 nm are arranged around a central rod. These 12defects rods are known as the cavity inner rods.

The cavity is connected with 3 waveguides (upper horizontal waveguide, lower horizontal waveguide and vertical waveguide) as shown in Fig. 1a. Upper horizontal waveguide has two ends point (left and right) as shown in figure, the left end point works as a bias port **B** and right end point acts as a input port **A**. The lower horizontal waveguide is a bypass waveguide.**O** is an output port of proposed NOT

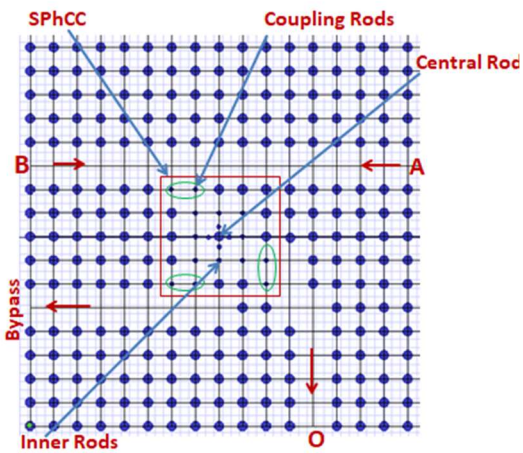

Fig. 1a: The layout of an optical NOT gate structure.

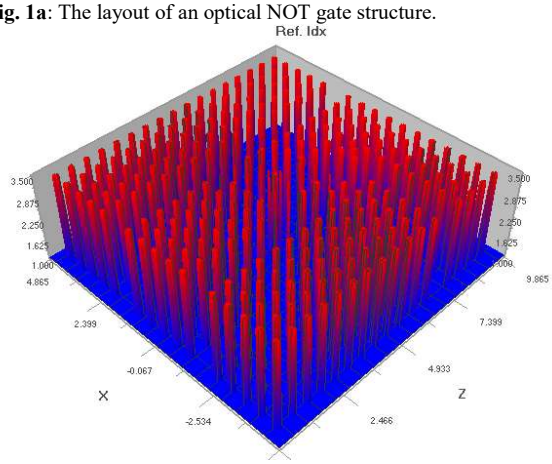

Fig. 1b: The refractive index profile (RIP) of NOT gate structure

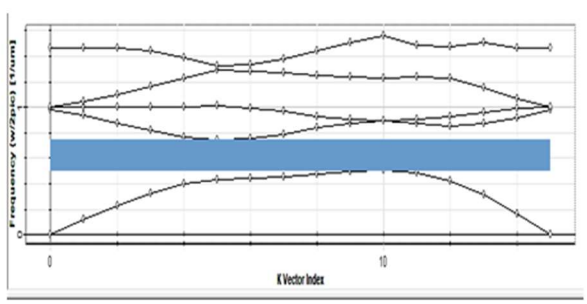

Fig.2: The photonic band diagram (PBD) of proposed NOT gate.

gate. Further radius of two coupling rods are reduced along three sides of the square cavity as shown. The complete schematic diagram of this optical NOT gate is depicted in **Fig. 1a**. The refractive index profile (RIP) of the gate is depicted in **Fig. 1b**.

The dielectric (Silicon) rods in the air are used in the planned structure, hence the PBG is computed in TE mode [18]. As shown in **Fig. 2**. PBG has a wavelength range of **0.505978 1/λ** to **0.747921 1/λ**,which relating in the range of **1337** to **1976 nm**. as depicted in **Fig. 2**. It indicates that such dielectric material is suitable for use in a CWDM system [18].

III. Operation of Optical NOT Gate

To demonstrate the role of structure, a simulation is done using the tool OptiFDTD. For simulation, we utilise a CW signal with a power of **Pa**[7] and a wavelength of 1.55 μmat the bias and input ports, respectively. We assume the following if power is equal or equivalent to **Pa** as logic **1,** or **ON** state, and power is zero or significantly below **Pa** as logic **0,** or **OFF** state[7].

Case 1: The bias port **B** is **ON** and input port **A** is **OFF** (**B=1**, **A=0**), the output port **O** becomes **1.00Pa** which corresponds to logic 1 or **ON** state. The snap shot of the electric field distribution (EFD) and normalized output power at the central wavelength ($1.55\ \mu m$) are shown in **Fig. 3a** and **3b**. **Fig. 3c** shows the time vs. normalized output power graph. The simulated electric field view (EFV) is shown in **Fig 3d**.

Case 2: Both the input ports are ON (**B=1**, **A=1**), therefore the input signal destructively interferes with the bias signal in the top waveguide, and the output t **O** becomes **0.17 Pa**, which corresponds to the logic **0** or **OFF** state. **Fig. 4a** and **4b** illustrate the distribution of the electric field as well as the normalised output power at the central wavelength. Figure 4c depicts the time vs normalised output graph.**Fig. 4d** shows the simulated EFV.

Table 1 shows the truth table of optical NOT gate.

The contrast ratio(CR) = $10\ log\frac{O(ON)}{O(OFF)}$[15] of suggested optical NOT gate is calculated as **7.69dB**.

This structure's response time (RT) is **150 fs**. According to Figure **3c** and **4c**, this value is calculated. Therefore data rate (bit rate) is **6.66 Tbps** because the data rate is reciprocal of response time.

TABLE 1: Truth table of optical NOT gate.

Port B	Port A	Port O	Output Logic
1	0	1.00Pa	1
1	1	0.17Pa	0

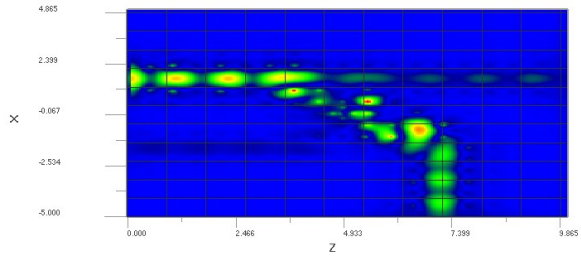

Fig. 3a

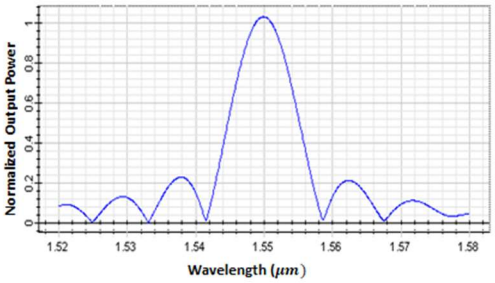

Fig.3b

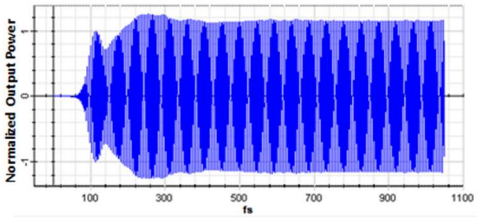

Fig.3c

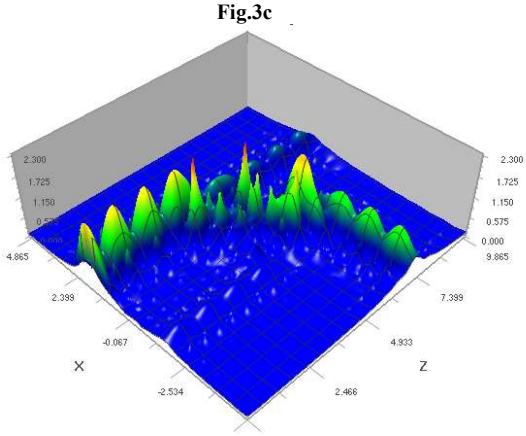

Fig.3d

Fig. 3: The NOT logic gate results when the bias is **ON** and the input signal is **OFF (a)** Electric field distribution **(b**) normalized output power at the central wavelength (1.55 µm)**(c)**Time vs. normalized output power graph (time evolving graph).**(d)** simulated electric field view (EFV).

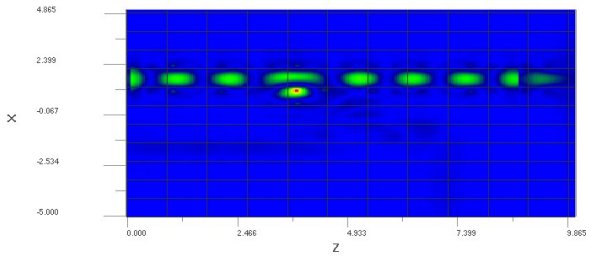

Fig.4a

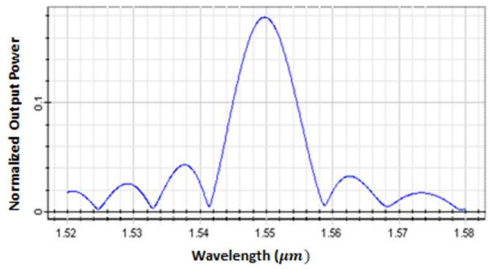

Fig.4b

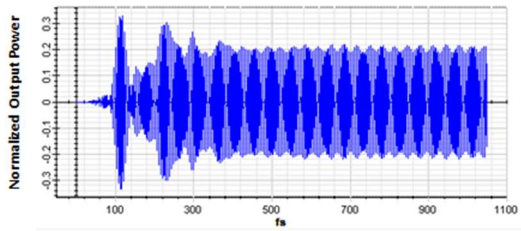

Fig.4c

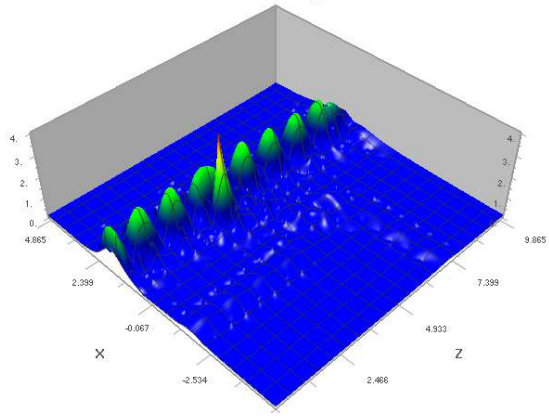

Fig.4d

Fig. 4: The outcome of an optical NOT logic gate when both the bias and input signals are **ON(a)** Electric field distribution **(b**) Normalized output power at the central wavelength (**1.55 µm)(c)** Time vs. normalized output power graph (time evolving graph).**(d)**simulated electric field view (EFV).

IV CONCLUSION

Based on SPhCC, an optical NOT is constructed. Numerical simulations successfully demonstrated by the 2D-FDTD method that the presented structure acts as an optical NOT gate. The response time, bit rate and contrast ratio for this NOT gate are $\mathbf{150}\,\boldsymbol{fs}$, $\mathbf{6.66}\,\boldsymbol{Tbps}$and $\mathbf{7.69}\,\boldsymbol{dB}$. The footprint of this structure is $\mathbf{89.98}\,\boldsymbol{\mu m^2}$which is compact. The suggested structure could be useful in designing of all optical computer system and processing circuits.

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